REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

I. STATUS OF THE CLAIMS

Claim 33 is canceled herein.

Claims 25-31, 34, and 35 are amended herein.

New claims 51-65 are added.

In view of the above, it is respectfully submitted that claims 25-32, 34, 35 and 51-65 are currently pending and under consideration.

II. REJECTION OF CLAIM 28 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

In item 3, on page 2 of the Office Action, claim 28 is rejected under 35 U.S.C. 112, second paragraph.

Claim 28 is amended herein to improve form and clearly recites that the amplifier amplifies the offset cancel voltage by a second amplification factor. See page 91 of the Applicants' specification.

In view of the above, it is respectfully submitted that the rejection is overcome.

III. REJECTION OF CLAIMS 25, 26, 33, AND 34 UNDER 35 U.S.C. § 102(E) AS BEING ANTICIPATED BY GUSMANO ET AL. (USP# 5,519,441)

In item 5, on page 2 of the Office Action, claims 25, 26, 33, and 34 are rejected as being anticipated by Gusmano et al.

The present invention as recited, for example, in claim 25 as amended herein, relates to a circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, comprising "a comparator receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result."

As described in column 8, lines 40-46, Gusmano discloses a comparator 33 which determines whether a black reference signal generated by the permanently darkened pixels 12 during the sub-scanning process has changed in comparison to the signal outputted by same

permanently darkened pixels 12 during power-up or the previous sub-scan.

It is respectfully submitted that the comparator of Gusmano functions differently from the claimed comparator. Moreover, Gusmano does not disclose or suggest the use of a comparator that receives a digital signal and determines whether the digital signal is within a predetermined offset value range, which defines allowable offset value range, to output a comparison result as recited in claim 25 of the present application. See page 84, lines 1-16 of the Applicants' specification.

Therefore, Gusmano does not disclose the features as recited in claim 25 of the present application.

Similar to claim 25, independent claims 26 and 27 recite "a comparator receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result" and independent claim 34 recites a method of "determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values." Therefore, Gusmano does not disclose the features recited in claims 26, 27, and 34 of the present application.

In view of the above, it is respectfully submitted that the rejection is overcome.

IV. REJECTION OF CLAIMS 29 AND 30 UNDER 35 U.S.C. § 102(E) AS BEING ANTICIPATED BY ZIPEROVICH (USP# 5,886,842)

In item 6, on page 3 of the Office Action, claims 29 and 30 are rejected as being anticipated by Ziperovich.

The present invention as recited, for example, in claim 29 as amended herein, relates to a circuit suitable for canceling an offset voltage, comprising "a sampling control circuit controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter."

Ziperovich discloses a parameter error extraction circuit which receives digital samples from an analog to digital converter, and which extracts parameter error values from digital samples. An averaging circuit is also disclosed for averaging the extracted parameter error values over an integral sub-multiple of the predetermined channel clock rate.

Ziperovich, however, fails to disclose a sampling control circuit controlling an A/D converter so that an interval between first and third sampling points and an interval between

second and fourth sampling points for an analog sinusoidal signal each, is 180 degrees as recited in claim 29 of the present application. See page 97, line 19 - page 98, line 4 of the Applicants' specification.

Therefore, Ziperovich does not disclose the features as recited in claim 29 of the present application.

Similar to claim 29, claim 30 recites "a sampling control circuit controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter."

We note the Examiner failed to comment on claim 35, which also recites "controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter." Therefore, Ziperovich does not disclose the features recited in claims 30 and 35 of the present application.

In view of the above, it is respectfully submitted that the rejection is overcome.

V. REJECTION OF CLAIM 27 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER GUSMANO ET AL. IN VIEW OF SATOH ET AL. (USP# 5,818,655)

In item 7, on page 4 of the Office Action, claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gusmano in view of Satoh.

Satoh discloses a signal processing circuit and information recording/reproducing apparatus using the same. Satoh does not teach or suggest the use of a comparator that receives a digital signal and determines whether the digital signal is within a predetermined offset value range, which defines allowable offset value range, to output a comparison result.

The comments in section III, above, also apply here.

Therefore, since Gusmano does not disclose the claimed comparator, it would not have been obvious to combine the teachings of Gusmano and Satoh to disclose the features recited in claim 27 of the present application.

Thus, Gusmano and Satoh, either alone or in combination, do not teach or suggest the features recited in claim 27 of the present application.

We note the Examiner failed to comment on claim 28, which depends from independent

claim 27. Nonetheless, for at least the reasons that claim 27 distinguishes over the cited prior art, it is respectfully submitted that claim 28 also distinguishes over the cited prior art.

In view of the above, it is respectfully submitted that the rejection is overcome.

VI. REJECTION OF CLAIMS 31 AND 32 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER ZIPEROVICH IN VIEW OF SATOH ET AL.

In item 8, on page 4 of the Office Action, claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziperovich in view of Satoh.

Again, Satoh discloses a signal processing circuit and information recording/reproducing apparatus using the same, but fails to teach or suggest a sampling control circuit as claimed in claim 31 of the present application.

The comments in section IV, above, also apply here.

Therefore, since Ziperovich does not disclose the claimed sampling control circuit, it would not have been obvious to combine the teachings of Ziperovich and Satoh to disclose the features recited in claim 31 of the present application.

Thus, Ziperovich and Satoh, either alone or in combination, do not teach or suggest the features recited in claim 31 of the present application.

Claim 32 depends from independent claim 31. Therefore, for at least the reasons that claim 31 distinguishes over the cited prior art, it is respectfully submitted that claim 32 also distinguishes over the cited prior art.

In view of the above, it is respectfully submitted that the rejection is overcome.

VII. NEW CLAIMS

Claims 51-54, 55-58, and 59-62 depend from independent claims 25, 26, and 27, respectively. Therefore, for at least the reasons the claims 25, 26, and 27 distinguish over the cited prior art, it is respectfully submitted that claims 51-54, 55-58, and 59-62 also distinguish over the cited prior art.

Claim 63 recites a method comprising "determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount," "accumulating said offset change amount," and "generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change

amount," which distinguishes over the cited prior art.

Further, claim 64 recites a circuit suitable for canceling an offset voltage of an A/D converter comprising "a comparator receiving said digital signal and for comparing a digital value of said digital signal with a predetermined offset value," "an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, wherein said addition result is initialized to a predetermined initial value," and "an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter," which distinguishes over the cited prior art.

Claim 65 recites "a comparator to receive said digital signal and compare a digital value of said digital signal with a predetermined offset value," "an arithmetic operation unit, connected to said comparator, to calculate a value of the changed amount of offset between the digital value and predetermined offset value, and output a result," and "an offset voltage generator, connected to said arithmetic operation unit, to generate an offset cancel voltage to cancel said offset voltage in accordance with the result, and supply said offset cancel voltage to said A/D converter," which distinguishes over the cited prior art.

In view of the above, it is respectfully submitted that claims 51-65 patentably distinguish over the cited prior art.

VIII. CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: December 19, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please CANCEL claim 33 without prejudice or disclaimer.

Please AMEND the claims in accordance with the following.

25. (ONCE AMENDED) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator [for] receiving said digital signal and [for comparing a digital value of said digital signal with a predetermined offset allowance value] determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result;

an arithmetic operation unit, connected to said comparator, [for] accumulating [a predetermined] an offset change amount and outputting an addition result based on said comparison result [when said digital value differs from said predetermined offset allowance values, wherein said addition result is initially determined by adding said predetermined offset change amount and a predetermined initial value]; and

an offset voltage generator, connected to said arithmetic operation unit, [for] generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and [for] supplying said offset cancel voltage to said A/D converter.

26. (ONCE AMENDED) A signal processor for receiving data information as an analog signal and processing said analog signal, comprising:

an A/D converter [for] converting said analog signal to a digital signal;

an offset cancel circuit, connected to said A/D converter, [for] supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit including,

a comparator [for] receiving said digital signal, and [for comparing a digital value of said digital signal with a predetermined offset allowance value] determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result;

an arithmetic operation unit, connected to said comparator, [for] accumulating [a predetermined] an offset change amount and [for] outputting an addition result based on said comparison result[, when said digital value differs from said predetermined offset allowance

value, said addition result being initially determined by adding said predetermined offset change amount and a predetermined initial value]; and

an offset voltage generator, connected to said arithmetic operation unit, [for] generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and [for] supplying said offset cancel voltage to said A/D converter.

27. (ONCE AMENDED) A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit [for] processing servo information; and

a data information processing circuit, connected to said servo information processing circuit, [for] receiving data information as an analog signal and [for] processing said analog signal, said data information processing circuit includes,

A) an A/D converter [for] receiving said analog signal from an input terminal and [for] converting said analog signal to a digital signal, to output said digital signal from an output terminal;

B) a switch connected to said input terminal of said A/D converter; and

C) an offset cancel circuit, connected between said input terminal and an output terminal of said A/D converter, [for] supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1) a control circuit, connected to said switch, [for] setting said switch off to inhibit supply of said analog signal to said A/D converter when said servo information processing circuit is performing a servo information process,

C2) a comparator connected to said comparator, [for] receiving said digital signal and [comparing a digital value of said digital signal with a predetermined offset allowance values] <u>determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values</u>, to output a comparison result,

C3) an arithmetic operation unit, connected to said comparator, [for] accumulating [a predetermined] <u>an</u> offset change amount and outputting an addition result based on said comparison result[, when said digital value differs from said predetermined offset allowance values, said addition result being initially determined by adding said predetermined offset change amount and a predetermined initial value], and

C4) an offset voltage generator connected to said arithmetic operation

unit, [for] generating an offset cancel voltage for canceling said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

28. (ONCE AMENDED) The signal processor according to claim 27, further comprising:

D) an amplifier, connected to said input terminal of said A/D converter and said control circuit, [for] amplifying said analog signal and said offset cancel voltage by a first amplification factor, wherein said amplifier [is capable of amplifying] amplifies said offset cancel voltage by a second amplification factor which is higher than said first amplification factor,

wherein said arithmetic operation unit has a reduced offset change amount inversely proportional to an increase ratio of said first amplification factor to said second amplification factor, and wherein said control circuit is connected to said comparator and said arithmetic operation unit, and

wherein when said digital value lies within [a range defined by] said predetermined offset [allowance] value range, said control circuit controls said amplifier in such a way as to amplify said offset cancel voltage by said second amplification factor and controls said arithmetic operation unit [in such a way as] to perform addition based on said reduced offset change amount.

29. (ONCE AMENDED) A circuit suitable for canceling an offset voltage of an A/D converter, said A/D converter samples an analog data signal including an analog sinusoidal signal in order to convert said analog data signal to a digital signal, said circuit comprising:

a sampling control circuit [for] controlling said A/D converter [in such a manner] so that an interval between first and third sampling [intervals] points and an interval between second and fourth sampling [intervals] points for said analog sinusoidal signal [become] each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order;

an arithmetic operation unit [for] receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and [for] computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter; and

an offset voltage generator [for] receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and [for] supplying said offset cancel voltage

to said A/D converter.

30. (ONCE AMENDED) A signal processor for receiving an analog data signal including an analog sinusoidal signal recorded on a recording medium, and processing said analog data signal, said signal processor comprising:

an A/D converter [for] converting said analog sinusoidal signal and said analog data signal to digital signals; and

an offset cancel circuit, connected to said A/D converter, [for] supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

a sampling control circuit [for] controlling said A/D converter [in such a manner] so that an interval between first and third sampling [intervals] points and an interval between second and fourth sampling [intervals] points for said analog sinusoidal signal [become] each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order;

an arithmetic operation unit [for] receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and [for] computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter; and

an offset voltage generator [for] receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and [for] supplying said offset cancel voltage to said A/D converter.

31. (ONCE AMENDED) A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit [for] processing servo information,

a data information processing circuit [for] receiving data information as an analog data signal including an analog sinusoidal signal and [for] processing said analog data signal, said data information processing circuit including,

A) an A/D converter [for] receiving said analog data signal from an input terminal and [for] converting said analog data signal to a digital signal to output said digital signal from an output terminal;

B) a switch connected to said input terminal of said A/D converter; and

C) an offset cancel circuit, connected between said input terminal and output terminal of said A/D converter, [for] supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1) a sampling control circuit [for] controlling said A/D converter [in such a manner] so that an interval between first and third sampling [intervals] points and an interval between second and fourth sampling [intervals] points for said analog sinusoidal signal [become] each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order,

C2) an arithmetic operation unit [for] receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and [for] computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter, and

C3) an offset voltage generator [for] receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and [for] supplying said offset cancel voltage to said A/D converter.

32. (UNAMENDED) The signal processor according to claim 31, wherein data information corresponding to said analog sinusoidal signal is a preamble pattern.

33. (CANCELED)

34. (ONCE AMENDED) A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising [the steps of]:

[comparing a digital value of said digital signal with a predetermined offset allowance value] determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount;

accumulating said offset change amount [when said digital value differs from said predetermined offset allowance value,];

stopping said accumulating, to determine an accumulated offset change amount, when said digital value lies within said predetermined offset allowance value[, and said offset change amount,]; and

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount.

35. (ONCE AMENDED) A method of canceling an offset voltage of an A/D converter for sampling an analog data signal including an analog sinusoidal signal to convert said analog data signal to a digital signal, said method comprising [the steps of]:

[using a control circuit for] controlling said A/D converter [in such a manner] so that an interval between first and third sampling [intervals] points and an interval between second and fourth sampling [intervals] points for said analog sinusoidal signal [become] each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first to fourth digital values are output from said A/D converter in a sampling order;

computing an average value of one of a set of said first and third digital values and a set of said second and fourth digital values, said obtained average value being an offset voltage value for said A/D converter; and

generating an offset cancel voltage to cancel said offset voltage in accordance with said offset voltage value.

Please ADD the following NEW claims:

51. (NEW) The circuit according to claim 25, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

52. (NEW) The circuit according to claim 25, wherein the arithmetic operation unit calculates the offset change amount on the basis of the comparison result and an offset unit change.

53. (NEW) The circuit according to claim 25, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

54. (NEW) The circuit according to claim 25, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

55. (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

56. (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit calculates the offset change amount on the basis of the comparison result and an offset unit change.

57. (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

58. (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

59. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

60. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit calculates the offset change amount on the basis of the comparison result and an offset unit change.

61. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

62. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

63. (NEW) A method of canceling an offset voltage of an A/D converter for

converting an analog signal to a digital signal, said method comprising:

determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount;

accumulating said offset change amount; and

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount.

64. (NEW) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator receiving said digital signal and for comparing a digital value of said digital signal with a predetermined offset value;

an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, wherein said addition result is initialized to a predetermined initial value; and

an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

65. (NEW) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator to receive said digital signal and compare a digital value of said digital signal with a predetermined offset value;

an arithmetic operation unit, connected to said comparator, to calculate a value of the changed amount of offset between the digital value and predetermined offset value, and output a result; and

an offset voltage generator, connected to said arithmetic operation unit, to generate an offset cancel voltage to cancel said offset voltage in accordance with the result, and supply said offset cancel voltage to said A/D converter.